IN THE CLAIMS

Please amend cancel claims 32-49. Please add new claims 50-67 as indicated below. The other claims are unchanged.

1. (Previously presented) A backplane interface adapter comprising:

at least one receiver that receives narrow input cells carrying packets of data;

at least one wide cell generator that generates encoded wide striped cells which include the packets of data from the narrow input cells; and

at least one transmitter that transmits the generated wide striped cells in multiple stripes to a switching fabric.

2. (Previously presented) The backplane interface adapter of claim 1, wherein each narrow input cell includes a destination slot identifier that identifies a slot of the switching fabric towards which the respective narrow input cell is being sent, and further comprising:

a traffic sorter coupled between said at least one receiver and said at least one wide cell generator, wherein said traffic sorter sorts said received narrow input cells based on said destination slot identifier.

3. (Original) The backplane interface adapter of claim 2, wherein said traffic sorter comprises a global/traffic sorter which sorts said received narrow input cells having a destination slot identifier that identifies a local destination slot from said received narrow input cells having destination slot identifiers that identify global destination slots across the switching fabric.

4. (Original) The backplane interface adapter of claim 3, wherein said traffic sorter further comprises a backplane sorter coupled to said global/traffic sorter, wherein said backplane sorter sorts said received narrow input cells having destination slot identifiers that identify global destination slots into groups based on the destination slot identifier.

5. (Original) The backplane interface adapter of claim 1, further comprising:

a plurality of stripe send queues coupled between said at least one wide cell generator and said at least one transmitter, wherein said at least one wide cell generator stores said generated wide striped cells in said plurality of stripe send queues.

6. (Original) The backplane interface adapter of claim 5, further comprising:

a switching fabric transmit arbitrator that arbitrates the order in which data stored in said stripe send queues is sent by the at least one transmitter to the switching fabric.

7. (Original) The backplane interface adapter of claim 6, wherein each stripe send queue stores a respective group of wide striped cells corresponding a respective originating source packet processor and a destination slot identifier.

8. (Original) The backplane interface adapter of claim 7, wherein each wide striped cell has one or more blocks across multiple stripes, and wherein during a cycle, said switching fabric transmit arbitrator selects a stripe send queue and pushes the next available block to said at least one transmitter.

9. (Original) The backplane interface adapter of claim 7, wherein each wide striped cell has one or more blocks across multiple stripes, and wherein during a cycle, said switching fabric transmit arbitrator selects a stripe send queue and pushes the next available block to said at least one transmitter.

10. (Previously presented) The backplane interface adapter of claim 1, wherein:

said at least one receiver comprises four deserializer receivers receiving said narrow input cells carrying packets of data in four serial data streams from four corresponding input serial pipes,

said multiple stripes comprise five stripes,

said at least one transmitter comprises five serializer transmitters, and

each serializer transmitter transmits one respective stripe of data of blocks of the generated wide striped cells over an backplane serial pipe to a respective crosspoint switch in the switching fabric.

11. (Original) The backplane interface adapter of claim 10, wherein each of said input serial pipes comprises a 10 gigabit/second serial pipe and said backplane serial pipe comprises a 50 gigabit/second serial pipe.

12. (Previously presented) The backplane interface adapter of claim 1, wherein each wide cell generator parses each narrow input cell, checks for control information indicating a start of packet, encodes one or more new wide striped cells until data from all narrow input cells of the packet is distributed into

the one or more new wide striped cells, and writes the one or more new wide striped cells into a plurality of send queues.

13. (Original) The backplane interface adapter of claim 1, wherein each wide cell generator encodes one or more new wide striped cells.

14. (Previously presented) The backplane interface adapter of claim 1, wherein each wide cell generator encodes an initial block of a start wide striped cell with initial cell encoding information.

15. (Original) The backplane interface adapter of claim 14, wherein said initial cell encoding information includes control information and state information, and said initial block of a start wide striped cell comprises five subblocks corresponding five stripes, and same wherein each subblock includes identical control information and identical state information.

16. (Original) The backplane interface adapter of claim 14, wherein each wide cell generator further distributes initial bytes of packet data into available space in said initial block of a first wide striped cell.

17. (Original) The backplane interface adapter of claim 16, wherein each wide cell generator distributes remaining bytes of packet data across one or more blocks in said first wide striped cell until an end of packet condition is reached or a maximum cell size is reached.

18. (Original) The backplane interface adapter of claim 17, wherein each wide cell generator further encodes an end wide

striped cell with end of packet information that varies depending upon a set of end of packet conditions including whether the end of packet occurs at the end of an initial block, at the end of the initial block, within a subsequent block, at a block boundary, or at a cell boundary.

19. (Previously presented) The backplane interface adapter of claim 1, wherein at the start of a packet, each wide cell generator encodes an initial twenty byte block of a start wide striped cell having twenty bytes of data distributed across five stripes as follows:

Block	Stripe 1	Stripe 2	Stripe 3	Stripe 4	Stripe 5
1	K0 STATE DATA0 DATAI	K0 STATE DATA2 DATA3	K0 STATE DATA4 DATA5	K0 STATE DATA6 DATA7	K0 STATE RES RES

where, K0 is one byte representing a special control character indicative of a cell start, STATE is one byte of state information, DATA0-DATA7 represent eight bytes of payload data, and RES is one reserved byte.

20. (Previously Presented) The backplane interface adapter of claim 1 , wherein each wide cell generator further encodes an end wide striped cell with end of packet information that varies depending upon the degree to which data has filled a wide striped cell.

21. (Original) The backplane interface adapter of claim 1, wherein each wide cell generator generates wide striped cells carrying no more than 148 bytes of payload data.

22. (Original) The backplane interface adapter of claim 1, further comprising:

at least one receiver that receives wide striped cells in multiple stripes from a switching fabric, the wide striped cells carrying packets of data;

a translator that translates said received wide striped cells to narrow input cells carrying the packets of data; and

at least one transmitter that transmits said narrow input cells to corresponding source packet processors.

23. (Original) The backplane interface adapter of claim 1, further comprising:

at least one wide striped cell receiver that receives subblocks of wide striped cells in multiple stripes from a switching fabric, the wide striped cells carrying packets of data across the multiple stripes and including source packet processor identifier and originating slot identifier information;

a stripe interface coupled to said at least one wide striped cell receiver;

a plurality of stripe receive synchronization queues coupled to said stripe interface, wherein said stripe interface sorts said received subblocks in each stripe based on originating slot identifier information and stores said sorted received subblocks in said stripe receive synchronization queues.

24. (Original) The backplane interface adapter of claim 23, further comprising:

an arbitrator;

a striped-based wide cell assembler, coupled to said

arbitrator, wherein said arbitrator arbitrates an order in which data stored in said stripe receive synchronization queues is sent to said striped-based wide cell assembler and said striped-based wide cell assembler assembles wide striped cells based on said received subblocks of data;

a translator, coupled to said striped-based wide cell assembler, wherein said translator translates the arbitrated received wide striped cells to narrow input cells carrying the packets of data;

a plurality of destination queues that store narrow cells sent by a local traffic sorter and said narrow cells translated by said translator;

a local destination transmit arbitrator that arbitrates an order in which data stored in said plurality of destination queues is sent to said at least one transmitter and

at least one transmitter that transmits said narrow input cells to corresponding source packet processors.

25. (Original) The backplane interface adapter of claim 1, wherein said at least one receiver comprises at least one deserializer receiver; and said at least one transmitter comprises at least one serializer transmitter.

26. (Original) A backplane interface adapter comprising:

at least one receiver that receives subblocks of wide striped cells in multiple stripes from a switching fabric, the wide striped cells carrying packets of data across the multiple stripes and including source packet processor identifier and originating slot identifier information;

a stripe interface coupled to said at least one receiver;

a plurality of stripe receive synchronization queues coupled to said stripe interface, wherein said stripe interface

sorts said received subblocks in each stripe based on source packet processor identifier and originating slot identifier information and stores said sorted received subblocks in said stripe receive synchronization queues.

27. (Original) The backplane interface adapter of claim 26, further comprising:

an arbitrator; and

a striped-based wide cell assembler, coupled to said arbitrator, wherein said arbitrator arbitrates an order in which data stored in said stripe receive synchronization queues is sent to said striped-based wide cell assembler and said striped-based wide cell assembler assembles wide striped cells based on said received subblocks of data.

28. (Original) The backplane interface adapter of claim 27, further comprising:

a translator, coupled to said striped-based wide cell assembler, wherein said translator translates the arbitrated received wide striped cells to narrow input cells carrying the packets of data; and

at least one transmitter that transmits said narrow input cells to corresponding source packet processors.

29. (Original) The backplane interface adapter of claim 28, further comprising:

a plurality of destination queues that store narrow cells sent by a local traffic sorter and said narrow cells translated by said translator; and

a local destination transmit arbitrator that arbitrates an order in which data stored in said plurality of destination queues is sent to said at least one transmitter.

30. (Original) The backplane interface adapter of claim 26, wherein said at least one receiver comprises at least one deserializer receiver; and said at least one transmitter comprises at least one serializer transmitter.

31. (Original) A backplane interface adapter comprising:

at least one deserializer receiver that receives narrow input cells carrying packets of data;

at least one wide cell generator that generates wide striped cells which include the packets of data from the narrow input cells;

at least one serializer transmitter that transmits the generated wide striped cells in multiple stripes to a switching fabric;

at least one deserializer receiver that receives wide striped cells in multiple stripes from a switching fabric, the wide striped cells carrying packets of data;

a translator that translates received wide striped cells to narrow cells carrying the packets of data; and

at least one narrow cell serializer transmitter that transmits narrow cells to corresponding source packet processors.

50. (New) A backplane interface adapter for interfacing with a switching fabric of a network switch, the network switch for switching packets in a network, the backplane interface adapter comprising:

at least one receiver that serially receives cells from the switching fabric via a full duplex serial link;

at least one transmitter that serially transmits cells to the switching fabric via a full duplex serial link;

wherein each said full duplex serial link is capable of handling full duplex traffic of at least 2.5 gigabits/second, and

wherein at least some of the cells comprise in-band state information and at least one byte of a said packet.

51. (New) The backplane interface adapter of claim 50, further comprising a second receiver that receives processed said packets from an at least 10 gigabit per second Ethernet packet processor of the network switch,

wherein the backplane interface adapter includes a sorter circuit that sorts the processed packets having a local destination slot from the processed packets having a global destination slot across the switching fabric.

52. (New) The backplane interface adapter of claim 50, wherein said state information comprises a destination slot identifier or a source slot identifier.

53. (New) The backplane interface adapter of claim 50, wherein said state information of a said cell received from the switching fabric comprises a source slot identifier.

54. (New) The backplane interface adapter of claim 50, wherein said state information of a said cell transmitted to the switching fabric comprises a destination slot identifier.

55. (New) The backplane interface adapter of claim 52 wherein at least some of the cells comprise the in-band state information, the at least one byte of a said packet, and in-band control information.

56. (New) The backplane interface adapter of claim 55, wherein the state information comprises payload state information that indicates a particular state of data in the cell.

57. (New) The backplane interface adapter of claim 52, wherein the state information comprises payload state information that indicates a particular state of data in the cell.

58. (New) The backplane interface adapter of claim 57, wherein the payload state information indicates a start of packet cell.

59. (New) The backplane interface adapter of claim 52, wherein at least some of the cells comprise the in-band state information, the at least one byte of a said packet, and information indicating an end of the packet.

60. (New) The backplane interface adapter of claim 51, wherein said state information of a said cell received from the switching fabric comprises a source slot identifier.

61. (New) The backplane interface adapter of claim 60, wherein at least some of the cells comprise the in-band state information, the at least one byte of a said packet, and in-band control information.

62. (New) The backplane interface adapter of claim 61, wherein the state information comprises payload state information that indicates a particular state of data in the cell.

63. (New) The backplane interface adapter of claim 51, wherein said state information of a said cell comprises a destination slot identifier.

64. (New) The backplane interface adapter of claim 63, wherein at least some of the cells comprise the in-band state information, the at least one byte of a said packet, and in-band control information.

65. (New) The backplane interface adapter of claim 64, wherein the state information comprises payload state information that indicates a particular state of data in the cell.

66. (New) The backplane interface adapter of claim 51, wherein said state information comprises a destination slot identifier or a source slot identifier.